

CLEAN VERSION OF PAR 2 ON PAGE 5 CONTINUING AS PAR 1 ON

PAGE 6

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The invention also relates to a device comprising a multi-layered circuitized sub assembly, and a semiconductor chip, preferably an optical chip coupled thereto. The sub assembly has two substantially parallel surfaces and at least one edge surface between the parallel surfaces. At least one conductive lead is embedded in the sub assembly generally parallel to the two parallel faces or surfaces, with one end forming electrical connection points. These points terminate in one or more electrical contact pads on said one edge surface. The semiconductor chip contains contacts electrically connected to the contact pads on the edge of the sub assembly. At least one active or passive device is mounted on a planar surface of the sub assembly and is in electrical contact with this conductive lead. The optical chip can be connected to the contact pads of the sub assembly using solder balls or any number of other connectors. The sub assembly may be formed into a plurality of laminates to make a stack. The laminates in the stack all have coplanar edge surfaces. They also have a stepped edge surface whereby each successive laminate in the stack is shorter than the laminate immediately there beneath. This serves to form an exposed planar surface or land on the lower laminate to accommodate an active or passive device that can be mounted on the exposed surfaces. One or more of the devices can be standard pin connectors that permit the device to be interfaced with a computer or suitable diagnostic device. One or more vias extend from each of the exposed planar surfaces of a laminate into the respective laminate to make contact with a conductive lead, thereby providing a connection between the semiconductor chip and the surface

mounted connector. The coplanar edge of the stack of laminates can form a right angle with respect to the planar surfaces of the laminate. Alternatively, each edge may form a bias angle less or greater than  $90^\circ$  with respect to the planar surface. This bias angle increases the size of the contact surface of the pad to which the component connection points can be made. The connection points on the edge surface may be exposed by any suitable means, such as cutting or shearing of the edge of the laminates collectively or individually, followed by stacking in such a manner as to make the edges coplanar.

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CLEAN VERSION OF PAR 3 ON PAGE 10 CONTINUING AS PAR 1 ON

PAGE 11

A2

Figure 3 is a view showing a VCSEL wafer 50 mounted to an optical coupler 52. A heat sink 54 with heat transfer fins 56 is joined to the coupler to remove generated heat from the laser wafer 50 and associated circuitry. Also shown is a fiber optic cable 58 having one end 60 adapted to be joined to the coupler 52. A handle 68 helps to attach and detach the cable from the coupler 52. The wafer 50 is typically about 1/8" by 1/16" in the planar direction, with a thickness of about 0.03". The individual fiber optic light sources are about 0.001" in diameter and are tightly spaced. Each of these light sources transmits optical data that must be relayed to a remote site to be read and/or analyzed. The optical data is transmitted through the laser wafer to a plurality of optical receivers (not shown) on the edge of a printed circuit core 10. The distal end 62 of the cable 58 is joined to the spectroscope that is used for diagnosis or exploration or for other medical purposes, in accordance with established medical protocols. The core is electrically joined to a conventional connector 70, such as those available from Amphenol or Molex, that is mounted on a planar surface 12 of the core. The wafer 50 is adapted to be optically connected through an optically transparent media to the edge 20 of the core 10 facing the wafer. Preferably, the media is an optically transparent encapsulant, such as a clear epoxy having the same or similar refractive index as that of the wafer. Air is not normally used for this purpose because of the loss of transmission across air gap, regardless of how small the air gap may be.

CLEAN VERSION OF PAR 3 ON PAGE 11 CONTINUING AS PAR 1 ONPAGE 12

A3

Another feature of the present invention involves the use of a stacked laminate of PCBs as shown in Figures 5 and 6. The substrate may be fabricated by building individual laminates with one or more conventional connectors on the planar surface of each laminate. Each laminated sub assembly is typically about 1/8" thick. A conventional connector is mounted on a planar surface 20a, 20b, 20c, etc of each laminated core 10a, 10b 10c. Each successive laminate 10 in the stack 24 is progressively shorter than the one below it, thereby accommodating a staggered array of connectors 60 as shown. After the stacked laminate is pressed together and cured, the edges 16 of the laminates opposite the connectors are sheared off to expose a matrix of connection points 72 to which electrical or optical contacts may be made. Each end can be cut at right angles to the planar surface of the stack or, to achieve a larger pad surface, the end can be cut at an angle of less than 90°, as shown, with a single laminated core in Figure 4. It should be understood that means other than shearing or cutting can be used to expose the ends of the conductive leads at the edge surfaces without departing from the intent of the present invention.